REMARKS

The Office Action dated June 7, 2005, has been received and reviewed.

Claims 1-33 are currently pending and under consideration in the above-referenced application. Each of claims 1-33 stands rejected.

Reconsideration of the above-referenced application is respectfully requested.

Rejections Under 35 U.S.C. § 103(a)

Claims 1-11 and 13-33 stand rejected under 35 U.S.C. § 103(a).

The standard for establishing and maintaining a rejection under 35 U.S.C. § 103(a) is set forth in M.P.E.P. § 706.02(j), which provides:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Fogal

Claims 1-4, 11, 13, 14, 16-18, 20-22, 24, 25, 31, and 32 stand rejected under 35 U.S.C. § 103(a) for reciting subject matter which is allegedly unpatentable over the subject matter taught in U.S. Patent 5,323,060 to Fogal et al. (hereinafter "Fogal").

Fogal teaches multi-chip modules (MCMs). An MCM according to Fogal includes an adhesive layer 38 interposed between two semiconductor chips 18 and 28 that have been superimposed relative to one another. *See, e.g.,* col. 2, lines 13-18; col. 2, lines 49-54. The adhesive layer 38 may be formed from an epoxy or an adhesive-coated tape. Col. 2 lines 67-68. The material may be electrically insulating. Col. 3, lines 8-9. The adhesive layer of Fogal has a thickness (*e.g.,* 0.008 inch) that is greater than a loop height of bonding wires 44 that protrude

above an active surface of the lower of the stacked semiconductor devices. Col. 2, lines 23-27; col. 2, lines 60-63; col. 3, lines 3-5.

Fogal does not provide any teaching or suggestion as to how the adhesive 38 thereof is formed. This point appears to have been acknowledged by the Office, which asserts that "predetermining an amount of material to be used in an assembly or a multi-chip module is . . . routine . . ." Office Action of June 7, 2005, page 5.

It is respectfully submitted that there are at least two reasons that a *prima facie* case of obviousness has not been established against any of claims 1-4, 11, 13, 14, 16-18, 20-22, 24, 25, 31, or 32.

First, it is respectfully submitted that Focal does not teach or suggest each and every element of any of claims 1-4, 11, 13, 14, 16-18, 20-22, 24, 25, 31, or 32. For example, Fogal explains that the adhesive 38 may be formed from a tape. Col. 2, lines 67-68. Such a tape would include an adhesive-coated dielectric film. Thus, the adhesive of such a tape would not space a second semiconductor device a predetermined distance from the surface of the first semiconductor device, as required by independent claim 1. Rather, the predetermined distance would be primarily defined by the thickness of the tape and to a much lesser extent by the thickness of the adhesive that has been coated onto the surfaces of the tape.

Fogal also teaches that an epoxy may be applied to a semiconductor device. *See* col. 2, lines 67-68. While it is conceded that a metered volume of the epoxy could be applied to a semiconductor device, Fogal does not teach or suggest applying a metered, or predetermined volume of epoxy or any other adhesive material to a semiconductor device. Further, the epoxy need not be applied to the surface of the first semiconductor device in substantially a predetermined volume for the resulting element to space a second semiconductor device a predetermined distance from the surface of the first semiconductor device and to define an adhesive perimeter 42. Instead, some viscous epoxy (of no particular volume) could be applied to the surface of the first semiconductor device, then the second semiconductor device positioned on the viscous epoxy and forced downward until the first and second semiconductor devices a spaced the predetermined distance apart from one another.

In any event, Fogal lacks any teaching or suggestion of "applying substantially a predetermined volume of adhesive material [to a] surface of a first semiconductor device" to "spac[e a] surface of [a] second semiconductor device [. . .] a predetermined distance apart from the [. . .] surface of the first semiconductor device," as recited in independent claims 1 and 16.

Second, without improperly relying upon the hindsight provided by the subject matter disclosed and claimed in the above-referenced application, one of ordinary skill in the art would not have been motivated to modify the teachings of Fogal in such a way as to render obvious the subject matter recited in any of claims 1-4, 11, 13, 14, 16-18, 20-22, 24, 25, 31, or 32. In particular, neither Fogal nor the art that was generally available before the earliest priority date for the above-referenced application suggests that application of substantially a predetermined volume of adhesive material to a surface of a semiconductor device would be useful for spacing the surface substantially a predetermined distance apart from another surface of another semiconductor device.

Therefore, a *prima facie* case of obviousness has not been established against either independent claim 1 or independent claim 16. As such, under 35 U.S.C. § 103(a), both of these claims recite subject matter which is allowable over the subject matter taught in Fogal.

Claims 2-4, 11, 13, and 14 are each allowable, among other reasons, for depending directly or indirectly from claim 1, which is allowable.

Claim 2 is further allowable since Fogal neither expressly nor inherently describes that the adhesive 38 thereof is applied to a surface over which bond wires 44 or other discrete conductive elements extend.

Claim 4 is further allowable because Fogal includes no express or inherent description of placing a semiconductor device on discrete conductive elements (*e.g.*, bond wires 44) that extend partially over a surface of another semiconductor device.

Each of claims 17, 18, 20-22, 24, 25, 31, and 32 is allowable, among other reasons, for depending directly or indirectly from claim 16, which is allowable.

Claim 25 is further allowable since Fogal does not expressly or inherently describe using adhesive material to draw one semiconductor device toward another until the two semiconductor devices are spaced substantially a set distance apart from one another.

Lee in View of Ogawa

Claims 1-4, 11, 13-18, 20-25, and 31-33 have been rejected under 35 U.S.C. § 103(a) for being drawn to subject matter that is assertedly unpatentable over teachings from U.S. Patent 6,388,313 to Lee et al. (hereinafter "Lee"), in view of the teachings of U.S. Patent 4,388,128 to Ogawa et al. (herinafter "Ogawa").

Lee teaches that an adhesive layer 23 may be coated onto a surface of a first semiconductor chip 21, including over gold wires 22 that extend partially over the first semiconductor chip 21. Col. 5, lines 22-32. "Wrapping" the gold wires 22 in this manner purportedly "prevent[s] the first set of gold wires 22 from being damaged by the mounting of the second semiconductor chip 24 onto the first semiconductor chip 21." Col. 5, lines 50-59. In view of this concern, it is presumed that the adhesive layer 23 absorbs some of the force that is applied to the second semiconductor chip 24 to adhere the same in place over the first semiconductor chip 21 and to space the first and second semiconductor chips 21 and 24 a desired distance apart from one another.

The teachings of Ogawa are likewise directed to a process in which movement of upper and lower stages 123 and 121 toward one another, rather than the volume of an adhesive material, spreads a drop of adhesive 124 to a desired thickness and spaces two chips 120 and 122 (a color image sensor and a color filter) a particular distance apart from one another. Col. 9, line 64, to col. 10, line 26.

It is respectfully submitted that there are at least two reasons that Lee and Ogawa do not support a *prima facie* case of obviousness against any of the claims of the above-referenced application.

First, one of ordinary skill in the art would not have been motivated to combine the teachings of Lee and Ogawa in the asserted manner. This is because the teachings of Lee are drawn to techniques for stacking semiconductor devices to form multi-chip modules, while

Ogawa teaches processes for bonding filters to color image sensors. Further, neither of these references includes any teaching or suggestion that the disclosed processes include application of substantially a predetermined volume of adhesive material to a semiconductor device. Instead, the teachings of Ogawa are limited to forcing two elements toward one another to spread adhesive material therebetween and, thus, to define a distance between the two semiconductor devices. Col. 9, line 64, to col. 10, line 26. The teachings of Lee appear to be similarly limited, as Lee indicates that an adhesive layer 23 prevents gold wires 22 from being damaged as a second semiconductor chip 24 is positioned over a first semiconductor chip 21. Col. 5, lines 50-59. As such techniques may be effected to space two elements a particular distance apart from one another regardless the amount of adhesive material that has been applied to one of the elements, is apparent that one of ordinary skill in the art would not have been motivated by either Lee or Ogawa to combine their teachings in the manner that has been asserted.

In fact, based on the limited disclosures of these references, as well as the lack of other art in support of the assertion that one of ordinary skill in the art would have been motivated to develop a method that includes applying substantially a predetermined volume of adhesive material to a semiconductor device, it appears that any such motivation could have only been improperly gleaned from the hindsight provided by the disclosure of the above-referenced application.

Second, neither Lee nor Ogawa teaches or suggests each and every element of either of independent claims 1 or 16. Specifically, Lee and Ogawa both lack any teaching or suggestion of applying substantially a predetermined volume of adhesive material to (or onto) at least a surface of a semiconductor device. Again, while both Lee and Ogawa disclose application of adhesive material to the surface of a semiconductor device, neither of these references teaches or suggests that the adhesive material is applied in a predetermined volume. Further, Lee and Ogawa both lack any teaching or suggestion that adhesive material spaces a surface of one semiconductor device a predetermined distance or substantially a predetermined distance apart from another surface of another semiconductor device. Instead, these references merely teach that the adhesive material is applied, that an element is positioned against the material, and that the element and a

semiconductor device are forced toward each other, which would define a distance that the semiconductor device and the element are spaced apart from one another.

In view of the foregoing, it is respectfully submitted that, under 35 U.S.C. § 103(a), independent claims 1 and 16 are both allowable over the subject matter taught in Lee and Ogawa.

Claims 2-4, 11, and 13-15 are each allowable, among other reasons, for depending directly or indirectly from claim 1, which is allowable.

Claim 4 is additionally allowable since Lee and Ogawa both lack any teaching or suggestion of placing a semiconductor device on discrete conductive elements. Rather, the teachings of Lee are limited to placing a second semiconductor chip 24 on adhesive 23 that coats gold wires 22.

Each of claims 17, 18, 20-25, and 31-33 is allowable, among other reasons, for depending directly or indirectly from claim 16, which is allowable.

Claim 25 is also allowable because Lee and Ogawa both lack any teaching or suggestion of using a predetermined volume of adhesive material to draw a semiconductor device toward a first semiconductor device.

Lee and Ogawa in View of Fujisawa

Claims 5-10, 19, and 26-30 are rejected under 35 U.S.C. § 103(a) for being directed to subject matter which is assertedly unpatentable over the subject matter taught in Lee, in view of teachings from Ogawa and, further, in view of the subject matter taught in U.S. Patent 5,801,439 to Fujisawa et al. (hereinafter "Fujisawa").

Claims 5-10 are each allowable, among other reasons, for depending directly or indirectly from claim 1, which is allowable.

Each of claims 19 and 26-30 is allowable, among other reasons, for depending directly or indirectly from claim 16, which is allowable.

It is further submitted that teachings from Lee, Ogawa, and Fujisawa cannot be relied upon to establish a *prima facie* case of obviousness against any of the claims of the above-referenced application. Specifically, it is respectfully submitted that one of ordinary skill

in the art would not have been motivated to combine the teachings of Lee, Ogawa, and Fujisawa in the manner that has been asserted.

The only possible motivation for one of ordinary skill in the art to combine the teachings of Lee, Ogawa, and Fujisawa would have been the fact that these references teach methods for stacking semiconductor devices. Nonetheless, the methods that are taught in Lee, Ogawa, and Fujisawa are completely different.

Lee teaches stacked multi-chip modules that include bare semiconductor devices in stacked arrangement, as well as methods for assembling such multi-chip modules.

Ogawa teaches methods for fabricating color image sensors; specifically, for bonding color filters to color image sensor chips.

The teachings of Fujisawa are directed to packaged semiconductor devices with leads that extend along at least portions of the exterior surfaces of the molded packages thereof. These packaged semiconductor devices may be stacked relative to one another and secured to each other with adhesive material. Corresponding leads of adjacent packages contact and communicate with one another.

Moreover, none of Lee, Ogawa, or Fujusawa teaches or suggests applying substantially a predetermined quantity of adhesive material to a surface of a semiconductor device, as required by all of the claims of the above-referenced application.

Therefore, it is apparent that the only source of motivation to combine the teachings of Lee, Ogawa, and Fujisawa would have been the disclosure of the above-referenced application, which would constitute improper hindsight.

Lee, Ogawa, and Fujisawa also lack any teaching or suggestion that one semiconductor device may be pushed away from another semiconductor device as adhesive material is introduced therebetween, as required by claim 29.

Additionally, none of Lee, Ogawa, or Fujisawa includes any teaching or suggestion that intermediate conductive elements may be coated with adhesive material as the adhesive material is introduced between two semiconductor devices.

For these reasons, it is respectfully submitted that a *prima facie* case of obviousness has not been established against any of claims 26-30, as would be required to maintain the 35 U.S.C. § 103(a) rejections of these claims.

Lin in View of Ogawa

Claims 1-4, 11, 13-18, 20-25, and 31-33 stand rejected under 35 U.S.C. § 103(a) for reciting subject matter which is purportedly unpatentable over teachings from U.S. Patent 6,333,562 to Lin (hereinafter "Lin"), in view of the teachings of Ogawa.

Lin teaches processes for separating the semiconductor dice of stacked multichip modules predetermined distances apart from one another. In these processes, conductive bumps 350 that include pillar protruding portions 350b are formed on bond pads of a lower semiconductor die 310. Col. 5, lines 9-14; FIG. 5; col. 6, lines 1-6; FIG. 8. An adhesive material is then introduced onto the active surface of the lower semiconductor die 310 to form an adhesive layer 340 thereon. Col. 5, lines 40-50; FIG. 7; col. 6, lines 23-28; FIG. 10. Another semiconductor die 320 is positioned over the lower semiconductor die 310, in contact with adhesive layer 340, and forced toward the lower semiconductor die 310 until the backside thereof contacts the pillar protruding portions 350b of bumps 350. *Id.*

Ogawa teaches methods for bonding color filters to color image sensors. These methods include applying adhesive to the sensors, then forcing the filters and the sensors toward one another.

It is respectfully submitted that there are at least two reasons that the teachings of these references do not support a *prima facie* case of obviousness against any of claims 1-4, 11, 13-18, 20-25, or 31-33.

First, one of ordinary skill in the art would not have been motivated to combine the teachings of these references in the manner that has been asserted. Specifically, one of ordinary skill in the art would not have been motivated to apply incorporate teachings that relate to bonding filters to color image sensors into techniques for assembling multi-chip modules. Moreover, neither Lin nor Ogawa actually teaches or suggests applying substantially a predetermined volume of adhesive material to at least a surface of a semiconductor device.

Instead, the teachings of both Lin and Ogawa are limited to forcing one element toward another following the application of adhesive material therebetween to define a distance between the two elements.

Based on the foregoing, it appears that any motivation to combine teachings from Lin and Ogawa could only have been improperly gleaned from the disclosure of the above-referenced application.

Second, neither Lin nor Ogawa teaches or suggests each and every element of any of claims 1-4, 11, 13-18, 20-25, and 31-33.

In contrast to the subject matter taught in Lin and Ogawa, independent claim 1 recites a method which includes "applying substantially a predetermined volume of adhesive material onto at least an active surface of a first semiconductor device . . .," which ultimately space the first semiconductor device apart from a second semiconductor device by substantially a predetermined distance.

Independent claim 16 is drawn to a method for forming a stacked MCM, which method includes "applying substantially a predetermined volume of adhesive material onto at least a surface of [a] first semiconductor device . . .," which ultimately results in the the surface of the first semiconductor device being spaced substantially a predetermined distance apart from an opposing surface of a second semiconductor device.

When the processes taught in Lin and Ogawa are employed, it does not matter how much (*i.e.,* the volume of) adhesive material that is applied to the surface of a semiconductor device. Rather, in Lin, the amount of force applied to an upper chip 320, the height of pillar protruding portions 350b that protrude from a lower chip 310, or a combination thereof dictates the distance that two stacked semiconductor devices (*i.e.,* chips 310 and 320) are spaced apart from one another. The amount of force applied to the filter 15 of Ogawa likewise defines the distance that the filter 15 is spaced apart from an underlying chip 16. Therefore, Lin and Ogawa, taken either separately or together, do not teach or suggest applying "substantially a predetermined quantity of adhesive material" to at least a surface of a semiconductor device or that substantially the predetermined quantity of adhesive material spacers the surface of the semiconductor device a predetermined distance or substantially a predetermined distance apart from another surface of

another semiconductor device, as is required by independent claims 1 and 16. As Lin and Ogawa do not teach or suggest each and every element of either independent claim 1 or independent claim 16, under 35 U.S.C. § 103(a), both of these claims recite subject matter which is allowable over the subject matter taught in Lin and Ogawa.

Each of claims 2-4, 11, and 13-15 is allowable, among other reasons, for depending directly or indirectly from claim 1, which is allowable.

Claim 4 is further allowable because Lin and Ogawa both lack any teaching or suggestion of placing a semiconductor device on discrete conductive elements (*e.g.,* bond wires) that extend partially over a surface of another semiconductor device.

Claims 17, 18, 20-25, and 31-33 are each allowable, among other reasons, for depending directly or indirectly from claim 16, which is allowable.

Claim 25 is further allowable since Lin and Ogawa do not teach or suggest using adhesive material to draw one semiconductor device toward another until the two semiconductor devices are spaced substantially a set distance apart from one another.

Withdrawal of the 35 U.S.C. § 103(a) rejections of claims 1-11 and 13-33 is respectfully requested.

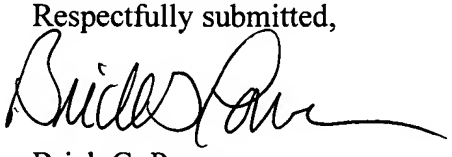
Claim 12

No specific grounds of rejection have been asserted against claim 12. It is, therefore, presumed that the subject matter recited in claim 12 is allowable over the art that has been cited in the above-referenced application.

CONCLUSION

It is respectfully submitted that each of claims 1-33 is allowable. An early notice of the allowability of each of these claims is respectfully solicited, as is an indication that the above-referenced application has been passed for issuance. If any issues preventing allowance of the above-referenced application remain which might be resolved by way of a telephone conference, the Office is kindly invited to contact the undersigned attorney.

Respectfully submitted,



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